UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/584,778	12/27/2006	Guoping Xiong	CU-4906 RJS	4950

26530 7590 06/11/2009

LADAS & PARRY LLP
224 SOUTH MICHIGAN AVENUE
SUITE 1600
CHICAGO, IL 60604

EXAMINER	
VERDERAMO III, RALPH	

ART UNIT	PAPER NUMBER
2186	

MAIL DATE	DELIVERY MODE
06/11/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/584,778	XIONG, GUOPING	
	Examiner	Art Unit	
	RALPH A. VERDERAMO III	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 June 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/14/2007 and 5/4/2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 1 is objected to because of the following informalities: Claim 1 is concluded with a semi-colon instead of a period. Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1 – 7 are rejected under 35 U.S.C. 102(b) as being anticipated by Klein et al. US Patent No. 5671439 (herein after referred to as Klein).

Regarding claim 1, Klein describes a data write-in method for flash memory (It will be appreciated that other physical mass storage devices may be used…Examples include…flash memories…(column 14, line 66 – column 15, line 5)), wherein the flash memory comprises at least two flash chips (Drive A and Drive B of FIG. 2), and the method includes: a. partitioning the physical blocks in the two flash chips to odd logical block addresses and even logical block addresses, respectively (means for alternately transferring even-numbered blocks of physical sectors between the on-board memory of the first drive and the main processing system and transferring odd-numbered blocks of physical sectors between the on-board memory of the second drive and the main processing system (column 4, lines 36 – 41)); b. receiving a data write-in

instruction and analyzing the beginning logical address corresponding to the writing operation from the data write-in instruction (The preferred routine preferably receives as input a starting logical sector START (column 8, lines 16 – 18). Retrieve xfer command 102 of FIG. 2); c. obtaining according to the beginning logical address the logical block address needed to be written, deciding the parity of the logical block address needed to be written, and selecting the corresponding flash chip between the two flash chips according to the parity of the logical block address needed to be written (Starting sector on drive A? 132 of FIG. 2); d. detecting whether the other flash chip needs to be programmed or erased after the programming or erase instruction is directed to the physical block corresponding to the logical block address in the corresponding flash chip (More? 142 of FIG. 2).

Regarding claim 2, Klein describes the data write-in method for flash memory according to claim 1 (see above), wherein it further comprises the following step: e. if the other flash chip needs to be programmed or erased, directing programming or erase instruction to the other flash chip (Drive B Ready? 146, Move Block of Data To/From Drive B 150 of FIG. 2).

Regarding claim 3, Klein describes the data write-in method for flash memory according to claim 1 (see above), wherein it further comprises the following step: f. if the other flash chip do not need to be programmed or erased, then judge whether the operation performed to the corresponding physical block in step d is finished (No path from More? 142 of FIG. 2).

Regarding claim 4, Klein describes the data write-in method for flash memory according to claim 3 (see above), wherein it further comprises: if the operation performed on the corresponding physical block has been finished, judge whether the data write-in instruction has been finished; if the operation performed to the corresponding physical block has not been finished, return to step d (More? 142 of FIG. 2).

Regarding claim 5, Klein describes the data write-in method for flash memory according to claim 3 (see above), wherein that: if the data write-in instruction has been finished, return to step b (New xfer command retrieved, restarting the method of FIG. 2); if the data write-in instruction has not been finished, return to step c (More? 142 and 152 Yes path of FIG. 2).

Regarding claim 6, Klein describes the data write-in method for flash memory according to claim 4 (see above), wherein that: the step b further comprises obtaining the number of sectors needed to be written from the data writing operation instruction (Calculate starting and total sectors for drives A & B 200 of FIG. 2).

Regarding claim 7, Klein describes the data write-in method for flash memory according to claim 6 (see above), wherein that: the method further comprises judging whether the data writing operation instruction has been finished by subtracting the number of written sectors from the number of need-to-be-written sectors (338 and 340 of FIG. 5(b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to RALPH A. VERDERAMO III whose telephone number is (571)270-1174. The examiner can normally be reached on M-Th 7:30 - 5, every other Friday 7:30-4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Ralph A Verderamo III/
Examiner, Art Unit 2186

rv
June 8, 2009

/Matt Kim/
Supervisory Patent Examiner, Art Unit 2186